

## **Integrated Design Flows : EDA's Answer to Rising Silicon Costs**

The EDA industry faces a unique paradox. Each new generation of silicon process node results in significant increases in design cost: at least 60% for engineering and 40% for manufacturing. And while finer process technologies are enabling the convergence of computer and communications, the complexity of these devices calls into question the feasibility of every chip, piece of software and end product. In addition, there is immense and intense pressure on chip designers to lower costs not only at the chip development stage, but beyond, at the manufacturing stage. The EDA industry cannot continue to meet the demand for increased functionality and lower costs with short-term responses of bug fixes and minor enhancements. Rather, a new approach to the way EDA tools are designed is needed.

There is only one way to adequately address current and emerging design challenges and provide a long-term solution that would result in significantly lower development and manufacturing costs and turnaround time for advanced designs. The EDA industry must provide tightly integrated design flows that eliminate iterations, address timing, area, power, and signal integrity and yield concurrently, and manage the complexity of nanometer designs. Without such a system, silicon design at nanometer process geometries will be economically infeasible.

Beyond the business rationale there are other reasons to create integrated flows. Electronic effects are interrelated so today's designers need to consider several critical parameters and objectives concurrently, including timing, power dissipation, signal integrity, design for test (DFT) and yield. All of these parameters are closely coupled—optimization of one affects the others. Their interrelationships require design tools that can perform concurrent optimization, which can only be accomplished when the tools are part of an integrated flow that uses a common data model. Concurrent optimization lets the designer solve problems that affect multiple design parameters. For example, fixing problems caused by IR drops on the chip, which can cause intra-chip variation in supply and ground voltage levels, results in both improved signal integrity and timing performance. An integrated flow enables more efficient design. First, it reduces the iterations between separate design operations such as synthesis and place-and-route. This not only reduces design time but also increases the probability of first-time silicon success. With an integrated tool flow from a single vendor, the chip design team can be more productive, since running an integrated suite is simpler than combining and running point tools from multiple EDA vendors.

Another economic advantage of a single-vendor integrated suite is the need for fewer tool licenses. Finally, an EDA suite from a single vendor is better equipped to deal with new design implementations, such as structured and platform ASICs. These implementations are becoming increasingly popular, since they reduce design time, design-iteration loops, risk, and cost compared to traditional ASIC and ASSP design flows.

Manufacturing costs can also be reduced with an integrated design automation flow. Close coupling of physical layout and logic synthesis operations result in better chip layouts, resulting in a smaller and less expensive chips. Yield is also increased because a smaller chip results in fewer vias and shorter average wire length, both of which reduce yield loss.

Another advantage of concurrent design-parameter optimization is reduced power dissipation. This has several benefits, including less power-induced performance variation across the chip, which enhances chip yield, and enables the use of less expensive IC packaging which reduces both chip and system cost.

Additional cost reductions can be achieved by integrating DFT into the flow, which results in higher yield through manufacturing test. Optimized test sequences reduce the time it takes to test the chip on expensive test equipment, further reducing manufacturing cost.

With a long-term vision, xxx developed its RTL-to-GDSII flow based on the facts stated above. This integrated flow uses a unified data model and embedded concurrent analysis and design-parameter optimization that has been proven to deliver 50-90% reduction in chip turnaround time, 10-15% smaller die sizes, and 15-35% lower power. As is often the case in the EDA and other industries, successful companies are the ones who can provide long-term solutions that reduce costs and improve results. Today in EDA, that solution is an integrated design flow.

**(The author of the article is -----)**